CLAIMS

1. A method for forming a trimmed gate in a transistor comprising the steps of:

forming a polysilicon portion of a gate conductor on a substrate having a semiconductor portion; and

trimming the polysilicon portion by a selective film growth method.

2. The method of claim 1, wherein the selective film growth method comprises selective surface nitridation.

3. The method of claim 1, wherein the selective film growth method comprises selective surface oxidation.

4. The method of claim 1, wherein the step of trimming the polysilicon portion further comprises selectively compensating n-channel and p-channel devices.

5. The method of claim 1, additionally comprising the step of at least partially removing the trimming film.

6. The method of claim 1, wherein the trimming film is anisotropically etched, forming gate conductor spacers.

7. The method of claim 1, wherein the trimming film is silicon-rich and the method further comprises the step of forming additional nitride or oxide layers on the trimming film.

8. The method of claim 2, wherein the step of trimming the gate conductor by selective surface nitridation comprises exposing structures formed on the semiconductor portion to 50-1000 expose pulses of laser irradiation with an energy fluence of 200-700 mJ/cm^2 in the presence of ammonia at a pressure of 10-1500 torr.

9. The method of claim 8, wherein the step of trimming the gate conductor by selective surface nitridation comprises exposing structures formed on the semiconductor portion to about 150 expose pulses of 308 nm laser irradiation with an energy fluence of 400-500 mJ/cm^2 in the presence of ammonia at a pressure of about 300-500 torr.

10. The method of claim 9, wherein ammonia is supplied at about 100 ccm/min.

11. The method of claim 3, wherein the step of trimming the gate conductor by selective surface oxidation comprises exposing structures formed on the semiconductor portion to 50-1000 expose pulses of laser irradiation with an energy fluence of 100-600 mJ/cm^2 in the presence of oxygen at a pressure of 1-760 torr.

12. The method of claim 11, wherein the step of trimming the gate conductor by selective surface oxidation comprises exposing structures formed on the semiconductor portion to about 150 expose pulses of 308 nm laser irradiation with an energy fluence of 200-400 mJ/cm^2 in the presence of oxygen at a pressure of about 100-300 torr.

13. The method of claim 12, wherein oxygen is supplied at about 100 ccm/min.

14. A method for forming selectively compensated semiconductor devices comprising the steps of:

forming a plurality of polysilicon portions of gate conductors on a substrate having a semiconductor portion;

masking at least one polysilicon portion intended for a n-channel device;

trimming at least one unmasked polysilicon portion intended for a p-channel device by a selective film growth method, wherein the extent of trimming is selected to accomplish device compensation of the p-channel and n-channel devices.

15. The method of claim 14, wherein the selective film growth method comprises selective surface nitridation.

16. The method of claim 14, wherein the selective film growth method comprises selective surface oxidation.

17. The method of claim 15, wherein the step of trimming the gate conductor by selective surface nitridation comprises exposing structures formed on the semiconductor portion to about 150 expose pulses of 308 nm laser irradiation with an energy fluence of 400-500 mJ/cm^2 in the presence of ammonia at a pressure of about 300-500 torr.

18. The method of claim 16, wherein the step of trimming the gate conductor by selective surface oxidation comprises exposing structures formed on the semiconductor portion to about 150 expose pulses of 308 nm laser irradiation with an energy fluence of 200-400 mJ/cm^2 in the presence of oxygen at a pressure of about 100-300 torr.

19. A transistor comprising a trimmed polysilicon portion of a gate conductor, wherein the trimming occurred by a selective film growth method.

20. The transistor of claim 19, wherein n-channel and p-channel devices were selectively compensated by the trimming.

21. The transistor of claim 19, wherein a sufficient portion of the trimming film is removed by anisotropic etching to provide gate conductor spacers.

22. The transistor of claim 19, wherein the trimming film is silicon-rich, allowing additional nitride or oxide layers to be formed.

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